

# Electron Spin Resonance Transistors for Quantum Computing in Silicon-Germanium Heterostructures

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We apply the full power of modern electronic band structure engineering and epitaxial heterostructures to design a transistor that can sense and control a single donor electron spin. Spin resonance transistors may form the technological basis for quantum information processing. One and two qubit operations are performed by applying a gate bias. The bias electric field pulls the electron wave function away from the dopant ion into layers of different alloy composition. Owing to the variation of the  $g$ -factor (Si:  $g=1.995$ , Ge:  $g=1.563$ ), this displacement changes the spin Zeeman energy, allowing single- qubit operations. By displacing the electron even further, the overlap with neighboring qubits is affected, which allows two-qubit operations. Certain Silicon-Germanium alloys allow a qubit spacing as large as 200 nm, which is well within the capabilities of current lithographic techniques. We discuss manufacturing limitations and issues regarding scaling up to a large size computer.

## I. INTRODUCTION

The development of efficient quantum algorithms for classically hard problems has generated interest in the construction of a quantum computer. A quantum computer uses superpositions of all possible input states. By exploiting this quantum parallelism, certain algorithms allow one to factorize [1] large integers with astounding speed, and rapidly search through large databases [2], and efficiently simulate quantum systems [3]. In the nearer term such devices could facilitate secure communication and distributed computing.

In any physical system, bit errors will occur during the computation. In quantum computing this is particularly catastrophic, because the errors cause decoherence [4] and can destroy the delicate superposition that needs to be preserved throughout the computation. With the discovery of quantum error correction [5] and fault-tolerant computing, in which these errors are continuously corrected without destroying the quantum information, the construction of a real computer has become a distinct possibility.

Even with the use of fault-tolerant computing a quantum computer engineer would still prefer a system that exhibits the smallest possible error rate on the qubits, the two level systems that hold the quantum information. In fact, Preskill [6] established a requirement for fault-tolerance; the ratio of the error rate to the computer clock rate has to be below a certain threshold.

Several systems have recently been proposed to obtain a physical implementation of a quantum computer. These systems include cold ion traps [7], nuclear magnetic resonance

(NMR) systems [8,9], all-optical logic gates [10,11], Josephson junctions [12], and semiconductor nanostructures [13]. Successful experimental demonstrations of one and two qubit computers were reported for trapped ion systems [14] and NMR systems [15].

Last year, Bruce Kane [16] proposed a very interesting and elegant design for a spin resonance transistor (SRT). He proposed to use the nuclear spins of  $^{31}\text{P}$  dopant atoms, embedded in a Silicon host, as the qubits. At low temperatures the dopant atoms do not ionize, and the donor electron remains bound to the  $^{31}\text{P}$  nucleus. The control over the qubits is established by placing a gate-electrode, the so-called A-gate, over each qubit. By biasing the A-gate, one can control the overlap of the bound electron with the nucleus and thus the hyperfine interaction between nuclear spin and electron spin, which allows controlled one-qubit rotations. A second attractive gate, a J-gate, decreases the potential barrier between neighboring qubits, and allows two nuclear spins to interact by electron exchange, which provides the required controlled qubit-qubit interaction.

The rate of loss of phase coherence between qubits in a quantum system is typically characterized by the dephasing time  $T_2$ . The  $T_2$  dephasing time of the nuclear spins in silicon is extremely long. The silicon host efficiently isolates the nuclear spins from disturbances [17]. A quantum computer based on semiconductors offers an attractive alternative to other physical implementations due to compactness, robustness, the potentially large number of qubits [18], and semiconductor compatibility with industrial scale processing. However, the required transistors are very small, since their size is related to the size of the Bohr radius of the dopant electron. Furthermore, after the calculation is completed Kane's SRT requires a sophisticated spin transfer between nuclei and electrons to measure the final quantum state.

We suggest using the full power of modern electronic band structure engineering and epitaxial growth techniques, to introduce a new, more practical, field effect SRT transistor design that might lend itself to a near term demonstration of qubits on a Silicon wafer. We alter Kane's approach by the implementation of these spin-resonance transistors in engineered Germanium/Silicon hetero- structures that have a controlled band structure. Si-Ge strained heterostructures, developed by IBM and other companies, are in the mainstream of Silicon technology, and are currently used for high frequency wireless communication transistors, and high-speed applications.

In Si-Ge hetero-structure layers we can control the effective mass of the donor electron to reduce the required lithographic precision, and to permit the SRT transistors to be as large as  $\approx 2000$  Å. The Bohr radius of a bound electron in Si-Ge can be much larger than in Silicon due to the very small effec-

tive mass in strained Si-Ge alloys, and their higher dielectric constant. This places the lithographic burden well within the practical range of electron beam lithography and almost within range of contemporary optical lithography.

Among the other simplifications, we will employ an electron spin, rather than a nuclear spin as the qubit. Owing to the difference in the electronic  $g$ -factor,  $g = 1.995$  for Si, and  $g = 1.563$  for Ge, the electron spin resonance transition can be readily tuned by an electrostatic gate on a compositionally modulated Si-Ge epilayer structure. By working with electron spins rather than nuclear spins, we avoid the requirement of a sophisticated spin transfer between electrons and nuclei, for read-in/read-out of quantum data. In addition, due to their higher Zeeman energy, electron spins will eventually permit a clock speed up to 1GHz compared to a speed  $\approx 75$ kHz projected for the nuclear spins. Likewise, isotopic purity is not critical for electron spins.

In order to read-out the final result of a quantum calculation we will need to be able to detect single electron charges. Individual electro-static charges are readily detected by conventional field effect transistors (FET's) at low temperatures, which obviates the need for the sophisticated single electron transistors (SET's). In this paper, we illustrate our design for an electron spin resonance transistor.

## II. ELECTRON SPIN DEPHASING TIME IN SILICON

Electron spins benefit from the same protective environment provided by the silicon host as nuclear spins. Indeed, the ESR line in doped Silicon at low temperatures turns out to be exceptionally clean and narrow compared to other ESR lines.

Feher [19–21] found that the Si:<sup>31</sup>P ESR line is inhomogeneously broadened by hyperfine interactions with neighboring nuclear spins. But the nuclear spin flip  $T_1$  relaxation times were measured [20] to be in the 1-10 hour range. Thus the nuclei can be regarded as effectively static on the time scales needed for quantum computing. Likewise the direct electron spin-flip  $T_1$  is also around [20] an hour.

On the question of the critical transverse  $T_2$  ESR dephasing linewidth there was only a little information. Feher and Gere studied some heavily doped n-Si:P samples, and found that the ESR linewidth actually narrowed [22] at high doping, down to a 1MHz linewidth at the 9GHz ESR frequency, for the heavy doping level,  $n=3 \cdot 10^{18}/\text{cm}^3$ . This unusual behavior was clearly the result of exchange narrowing of the hyperfine inhomogeneity. For quantum computing, the issue is the linewidth of a single electron spin transition, rather than a heavily doped inhomogeneous ensemble.

Thus the outlook was optimistic. If the linewidth is only 1MHz at such a high doping level, and is due to exchange with neighboring electrons, then the linewidth would surely be much narrower at lower doping levels, and especially for one isolated electron. Indeed that was confirmed by Chiba and Hirai [23] who measured a  $1/2\pi T_2$  linewidth of only  $\approx 1$ kHz at a doping of  $10^{16}$  Phosphorus ions per  $\text{cm}^3$ , by the very reliable spin-echo technique. The residual linewidth was interpreted as being due to spin diffusion via the nuclear spins.

Indeed the linewidth was shown [24] to narrow further in isotopically purified, 0 spin, Si<sup>28</sup>, making the  $T_2$  dephasing even slower. The observed 1kHz linewidth at  $n=10^{16}/\text{cm}^3$  is already narrow enough, in relation to the 9GHz ESR frequency to satisfy Preskill's criterion [6] for fault tolerant computing.

The electron spin resonance (ESR) of a bound donor in Silicon provides many advantages: Firstly, in a magnetic field of 2 Tesla, the ESR resonance frequency is  $\approx 56$ GHz, easily allowing qubit operations at up to  $\approx 1$ GHz. This is comparable to the clock speed of ordinary computers, and is consistent with the precision of electronic control signals that are likely to be available. Secondly, at temperatures below 1K, the electron spins are fully polarized allowing a reproducible starting point for the computation. And finally, for electron spins isotopic purity is not compulsory since the nuclear spin inhomogeneity remains frozen at low temperatures.

## III. SRT TRANSISTOR SIZE AND LITHOGRAPHIC CRITICAL DIMENSION

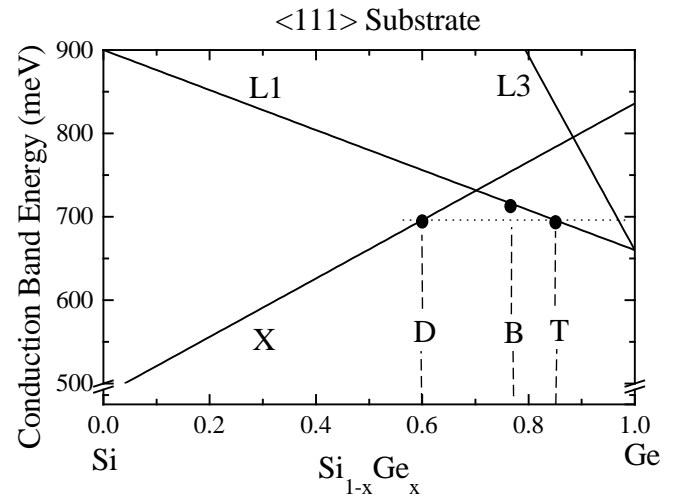


FIG. 1. The conduction band energy in Si-Ge alloys, compositionally strained in the  $\langle 111 \rangle$  direction, from neutral strain at 100% Ge. The X-valley has 6 minima that remain degenerate. The L-valley has 4 minima that are split between L1 and L3. The conduction band changes from the X- to L1-character at a composition of Si<sub>0.3</sub>Ge<sub>0.7</sub>. At this band transformation, the  $xy$ -effective mass becomes relatively light, the Bohr radius increases, and the  $g$ -factor drops from  $g \approx 1.995$  to  $g \approx 1.563$ . The fractional compositions D, T, and B, will be used in our band structure engineered, spin resonance transistor.

The Bohr radius of the bound carrier wave function regulates the size scale of Spin Resonance Transistors. In semiconductors the Bohr radius is much larger than in vacuum, since the Coulomb force is screened by the dielectric constant, and the effective mass is much smaller. Thus the bound carrier roams farther. The Bohr radius is:  $a_B = \epsilon \frac{m_0}{m^*} (\frac{\hbar^2}{m_0 q^2})$  in the semiconductor, where  $\frac{m^*}{m_0}$  is the effective mass relative to the free electron mass,  $\epsilon$  is the dielectric constant,  $\epsilon = 16$  for Ge,

and  $\epsilon = 12$  for Si and the quantity in parenthesis is the Bohr radius in vacuum.

It is common in Si-Ge alloys to have strain available as an engineering parameter. Strain engineering of valence band masses has been very successful, and is used [25] in virtually all modern semiconductor lasers. In the conduction band, strain splits the multiple conduction band valley energies, allowing one valley to become the dominant lowest energy conduction band. If that valley also happens to be correctly aligned, the donor wave functions can have a low mass moving in the plane of the silicon wafer, and a high mass perpendicular to the wafer surface. That is exactly what we are looking for in spin resonance transistors. We want large wave functions in the directions parallel to the wafer surface, in order to relax the lithographic precision that would have been demanded if the Bohr radius were small.

In Si-rich alloys there are 6 conduction band minima, in the 6 cubic directions, that are frequently labeled as the X-directions. In Ge-rich alloys, there are 4 conduction minima located at the  $\langle 111 \rangle$  faces of the Brillouin Zone, labeled L. The Ge-rich case is particularly interesting, since it has a conduction band mass of only  $0.082m_0$  in the transverse direction. Under  $\langle 111 \rangle$  strain the 4 conduction band valleys split so that one of them is lowest in energy and is labeled L1. The other 3 valleys remain degenerate and are labeled L3. Figure 1 shows the conduction band structure in the Si-Ge alloys, grown compositionally strained in the  $\langle 111 \rangle$  direction, with neutral strain at 100% Ge, as adapted from a more complete set of band structures from Wang *et al* [26].

The Hydrogenic Schrodinger equation for anisotropic effective mass,  $m_{xy}$  in the plane of the wafer, and  $m_z$  perpendicular to the plane of the wafer, has been solved for arbitrary values of  $m_{xy}/m_z$  by Schindlmayr [27]. The Bohr radius in the  $xy$ -plane is influenced by both effective masses:

$$a_{B,xy} = \frac{2\epsilon}{3\pi} \frac{2 + (m_{xy}/m_z)^{1/3}}{m_{xy}} a_B^0 \quad (1)$$

with  $a_B^0$  the Bohr radius of a free hydrogen atom and  $m_{xy} \ll m_z$  is assumed, as is appropriate for the  $z$ -oriented Si and Ge conduction band ellipsoids. The Bohr radius in the heavy mass direction,  $a_{B,z}$  is given by  $a_{B,z} = (\frac{m_{xy}}{m_z})^{1/3} a_{B,xy}$ . Using the actual masses and the exact formula [27], we give the Bohr radii in Si and Ge for  $z$ -oriented conduction band ellipsoids in Table I.

In Table I, special note should be taken of the Bohr radius =  $64\text{\AA}$  for  $\langle 111 \rangle$  strained Ge-rich alloys in which the L1 band minimum forms the conduction band. At that orientation, the X-band minima in Si-rich alloys would have a Bohr radius of only  $\approx 20\text{\AA}$ . Thus we achieve over a factor 3 increase in the transistor spacing by using a Ge-rich layer.

TABLE I. Conduction band effective masses relative to  $m_0$ , and the corresponding Bohr radii in Si and Ge.

material	$\epsilon$	$m_{xy}$	$m_z$	$a_{B,xy}$	$a_{B,z}$
Germanium	16	0.082	1.59	64 $\text{\AA}$	24 $\text{\AA}$
Silicon	12	0.191	0.916	25 $\text{\AA}$	15 $\text{\AA}$

Given that the exchange interaction is a dominant influence among the donor spins, we make the point that Preskill's de-coherence criterion can be redefined [28] as the on/off ratio of the spin-spin interaction, as induced by the transistor gates. The actual required transistor spacing is set by the need for the weakest possible exchange interaction when the 2-qubit interaction is off, and a strong exchange interaction when 2-qubit interactions are turned on. The exchange energy  $4J$  between hydrogenic wave functions determines both time scales:

$$\frac{4J(r)}{h} \approx 1.6 \frac{q^2}{\epsilon a_B} \left(\frac{r}{a_B}\right)^{5/2} \exp \frac{-2r}{a_B} \quad (2)$$

If we require the exchange energy in the off-state to be less than the measured [23]  $T_2$  dephasing linewidth  $\approx 1\text{kHz}$ , then the donor ions would have to be about 29 Bohr radii apart, allowing a spacing of about  $2000\text{\AA}$ . Such critical dimensions are well within the range that can be produced by electron beam lithography.

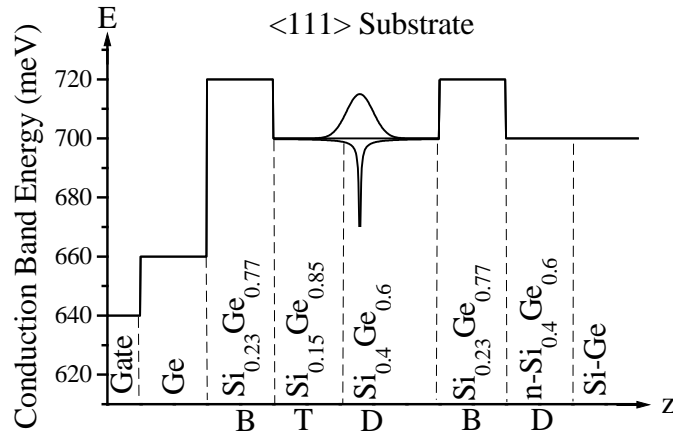


FIG. 2. The band structure diagram for the proposed spin-resonance transistor, showing the Coulombic potential well of the donor ion in the  $\text{Si}_{0.4}\text{Ge}_{0.6}$  D-layer where the conduction band minimum is X-like. The hydrogenic wave function partly overlaps the  $\text{Si}_{0.15}\text{Ge}_{0.85}$  T-layer where the conduction band minimum is L-like. The donor electron is confined by the two  $\text{Si}_{0.23}\text{Ge}_{0.77}$  B-barrier layers. The epi-layer thicknesses are not to scale.

Later we will show that by gate-controlled Stark distortion of the hydrogenic wave functions, the Bohr radius can be further increased, switching on the 2-qubit interactions. This will be accomplished by band structure engineering using only one ordinary electrostatic gate on the transistors, rather than 2 gates required by Kane.

#### IV. GATE CONTROLLED SINGLE QUBIT ROTATIONS IN THE SPIN-RESONANCE TRANSISTOR

The essence of a spin-resonance transistor (SRT) qubit is that a gate electrode should control the spin-resonance fre-

quency. By tuning this frequency with respect to the frequency of a constant radiation field, that is always present while the computer is being operated, single qubit rotations can be readily implemented on the electron spin. A band structure diagram for the SRT is shown in Figure 2. We rely on the difference in electronic  $g$ -factor,  $g = 1.995$  for Si-rich alloys, and  $g = 1.563$  for Ge-rich alloys. Thus, the electron spin resonance transition can be readily tuned by an electrostatic gate on a compositionally modulated Si-Ge epilayer structure, such as shown in Figure 3. In a study of the composition dependence of the  $g$ -factor in Si-Ge alloys, Vollmer and Geist [29] showed that the  $g$ -factor is most influenced by the band structure crossover from X to L1 at a composition of  $\text{Si}_{0.3}\text{Ge}_{0.7}$ , and hardly at all by compositional changes away from that crossover.

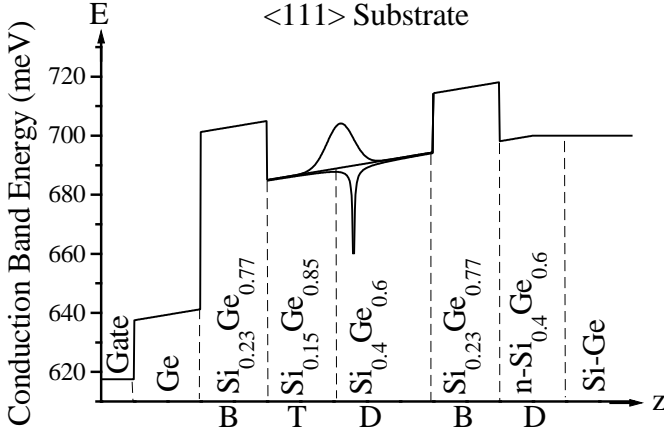


FIG. 3. The donor electron wave function is electrostatically attracted toward the  $\text{Si}_{0.15}\text{Ge}_{0.85}$  T-layer where the conduction band minimum is L1-like. There it will experience a smaller  $g$ -factor, that is gate tunable. The actual  $g$ -factor will be a weighted average between the D- and T-layers.

The  $^{31}\text{P}$  dopant atoms are positioned in the  $\text{Si}_{0.4}\text{Ge}_{0.6}$  D-layer, a composition which is to the left of the crossover in Figure 1. By electrostatically attracting the electron wave function into the  $\text{Si}_{0.15}\text{Ge}_{0.85}$  T-layer, the spin resonance can be tuned very substantially.

The two barrier layers of composition  $\text{Si}_{0.23}\text{Ge}_{0.77}$ , labeled B in Figure 2, have a conduction band structure as indicated in Figure 1. They have an L1-like conduction band minimum, to the right of X-L1 band structure cross-over, and thus have the same  $g$ -factor as the  $\text{Si}_{0.15}\text{Ge}_{0.85}$  T layer. The purpose of the B layers is to confine the donor electrons and prevent them from tunneling away and becoming lost. The energy height of the barrier need only be comparable to the donor binding energy,  $\approx 20\text{meV}$  to fulfil this task. On the other hand the  $\text{Si}_{0.4}\text{Ge}_{0.6}$  D-layer and the  $\text{Si}_{0.15}\text{Ge}_{0.85}$  T-layer should have no energy barrier between them so that the  $g$ -factor can be freely tuned. Thus the D layer and the T layer are selected at compositions straddling the X-L1 crossover in Figure 1, so that their respective conduction band energies  $E_D$  and  $E_T$  are the same. A schematic tuning curve for our proposed spin resonance transistor is shown in Figure 4.

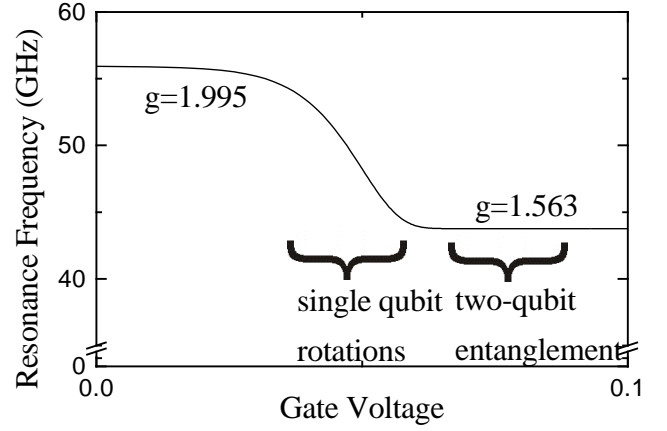


FIG. 4. A schematic of the dependence of the spin resonance frequency on the transistor gate voltage. As the electrons are pulled toward the positive gate electrode and into the more Ge-rich alloy compositions, the hetero-barrier B-layer prevents the donors from becoming completely ionized. At intermediate gate voltages, the  $g$ -factor can be tuned from  $g=1.995$  to  $g=1.563$ . The frequencies on the vertical axis correspond to a magnetic field of 2 Tesla. The two-qubit tuning range will be explained in the next section.

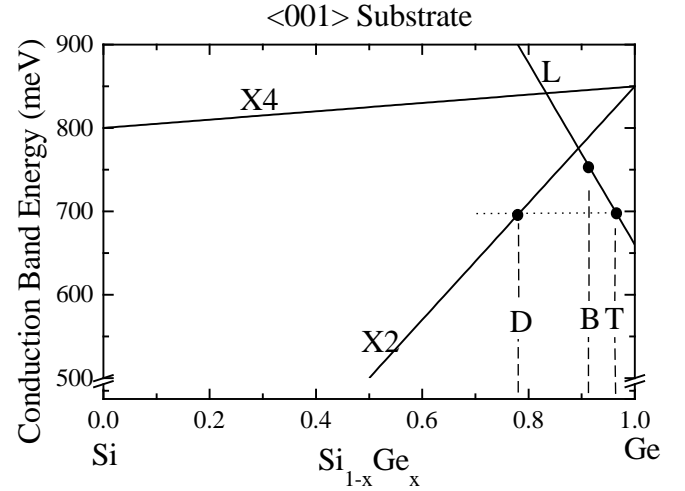


FIG. 5. The conduction band energy in Si-Ge alloys, compositionally strained in the  $\langle 001 \rangle$  direction, from neutral strain at 100%Ge. The L-valley has 4 minima that remain degenerate. The X-valley has 6 minima along the cubic directions, that are split between X4 and X2. The compositions D, T, and B are much less strained than in the  $\langle 111 \rangle$  case, and allow for higher barrier heights to confine the dopant electron.

As the spin resonance transistors are tuned in and out of resonance with the radiofrequency field the electron spin can be flipped, or subjected to a phase change. The wave function distortion during tuning is shown for the left side transistor in Figure 7. The confinement barriers of composition B

$\text{Si}_{0.23}\text{Ge}_{0.77}$ , play an important role. They must confine the qubit donor electrons for long periods of time, lest the carriers and their quantum information be lost. For that purpose the B-barrier layers each need to be about  $200\text{\AA}$  thick, for a carrier lifetime comparable to the  $\approx 1\text{hour}$   $T_1$  spin-lattice relaxation for electron spin flips. The two layers combined would total about  $400\text{\AA}$ , well within the practical strain limit [30] of  $\approx 1000\text{\AA}$  for growth of a 23% compositionally strained alloy. The D and T layers have thicknesses similar to the  $a_{B,z}$  vertical Bohr radius and contribute only slightly to the strain burden.

If one uses alloys grown in the  $\langle 001 \rangle$  direction instead, the numbers become even more favorable. Figure 5 shows the conduction band structure in the Si-Ge alloys, grown in the  $\langle 001 \rangle$  direction [30], compositionally strained from neutral strain at 100% Ge. In this growth direction, the L band remains unsplit, and the X band splits up into a doubly degenerate X2 and a quadruply degenerate X4 band. As can be seen, the conduction band energy changes much more rapidly as a function of alloy composition for the  $\langle 001 \rangle$  growth direction. Moreover, the X2 and the L bands cross over at approximately 90% Ge instead of 70% as in the Ge  $\langle 111 \rangle$  case. This allows us to select alloys with much lower strain, while obtaining a barrier height of 50 meV, more than twice the barrier height obtained in the  $\langle 111 \rangle$  direction.

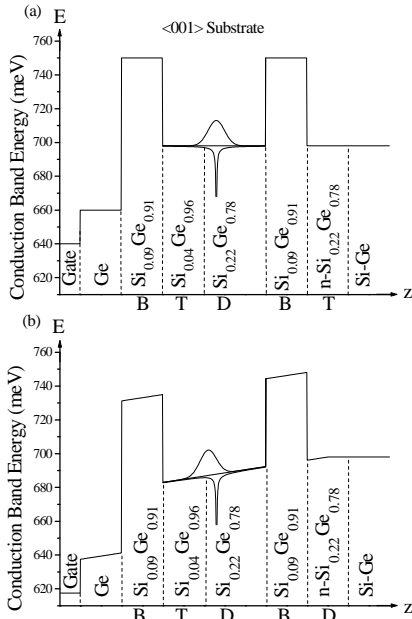


FIG. 6. The band structure diagram for the spin-resonance transistor, with epilayers grown in the  $\langle 001 \rangle$  direction. Both the unbiased (a) and the biased case (b) are shown. The conduction band energies allow the selection of layers with composition D, T, and B such that the confining barrier height is increased to 50 meV, while the strain in the layers is reduced, compared to the  $\langle 111 \rangle$  orientation. The epi-layer thicknesses are not to scale.

Consequently the layers can be made thinner while still pre-

venting tunneling of the dopant electron and the strain tolerance is significantly improved. The corresponding band structure diagram for the  $\langle 001 \rangle$  oriented SRT is shown in Figure 6.

The use of the  $\langle 001 \rangle$  growth direction comes at the expense of an increased effective mass in the  $xy$ -plane and a lighter mass in the  $z$ -direction. The conduction band ellipsoid pointing in the  $\langle 111 \rangle$  direction is  $55^\circ$  away from the  $\langle 001 \rangle$  direction and thus the  $z$ -direction no longer coincides with the heavy mass direction ( $\langle 111 \rangle$ ). Some of the heavy mass is transferred into the  $xy$ -plane, resulting in shorter Bohr radii. However, the lightest mass in Ge is equal to the heaviest mass in Si (see Table I). Therefore, the Ge-rich layer will always remain the layer with Bohr radii in the  $xy$ -direction which are at least as large as those in the Si-rich layer. Therefore Ge-rich layers will again perform the function of the tuning T-layer, and the barrier B-layer for structures grown in the  $\langle 001 \rangle$  as they did for the  $\langle 111 \rangle$  direction.

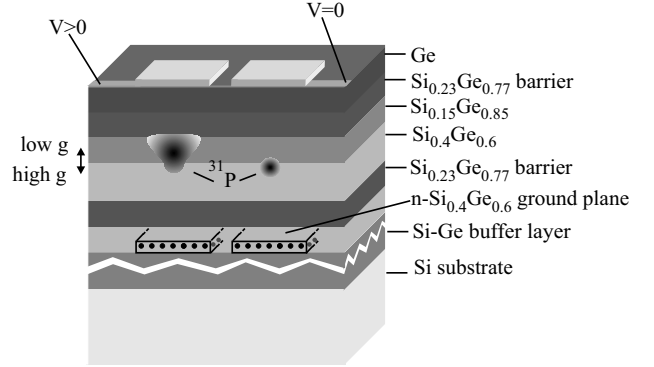


FIG. 7. The left transistor gate is biased  $V > 0$  producing single qubit unitary transformations in the left SRT. The right gate is unbiased,  $V = 0$ . The  $n\text{-Si}_{0.4}\text{Ge}_{0.6}$  ground plane is counter-electrode to the gate, and it also acts as an FET channel for sensing the spin.

## V. TWO-QUBIT INTERACTIONS

The spin resonance transistors must be spaced far enough apart, that they will not produce phase errors in one another. At the same time it is necessary to allow wave function overlap for the exchange interaction to activate the 2-qubit interactions. These are needed to produce for example a Controlled NOT (CNOT) gate, which is required to build a universal set of quantum logic gates. To achieve this we rely on our ability to tune the Bohr radius of the donors in the  $xy$ -direction parallel to the semiconductor surface.

The Bohr radius  $a_B$  of a hydrogen-like donor increases with decreasing binding energy. A famous example is excitons confined in a 2-d flat quantum well: The excitonic binding energy is four times greater [31] than it would be in 3 dimensions. The reason is that spatial confinement forces the electron to spend more time near the positive charge, and it experiences tighter binding. Accordingly the Bohr radius is diminished. For the same reason, confinement by heavy mass in the  $z$ -direction reduces the Bohr radius in the  $xy$ -plane as can be seen from Equation 1. Without this reduction the ef-

fective mass in the  $xy$ -direction in strained  $\langle 111 \rangle$  Ge would even be higher.

Our technique for 2-qubit interactions does not require any J-gates. By increasing the gate voltage, we pull the electron wave function away from the positive ion, to reduce the binding energy, and increase the wave function overlap between electrons bound to neighboring dopant ions. As shown in Figure 3, the electrons can be electro-statically attracted to one of the barriers formed by the  $\text{Si}_{0.23}\text{Ge}_{0.77}$  B-composition layer, forming a type of modulation doped channel in the  $xy$  plane. The binding energy to the positive ions is greatly weakened, since the electrons are spending most of their time near the  $\text{Si}_{0.23}\text{Ge}_{0.77}$  B-barrier. Consequently the Coulomb potential becomes weakened to the following form:

$$V = -\frac{q}{\sqrt{r^2 + d^2}} \quad (3)$$

where  $r^2 = x^2 + y^2$  is the horizontal distance from the donor ion, squared, and  $d$  is the vertical spacing from the barrier to the donor ion, and  $q$  is the electronic charge. Thus by adjusting the vertical depth of the ion,  $d$ , the Coulomb potential can be made as weak as desired. The weak Coulomb binding energy implies a large Bohr radius. The large radius permits a substantial wave function overlap in the  $xy$ -plane along the B-barrier layer, and a substantial 2-qubit exchange interaction. It should be possible to tune from negligible exchange interaction, all the way to a conducting metallic 2-d electron gas, by adjusting the vertical spacing  $d$ .

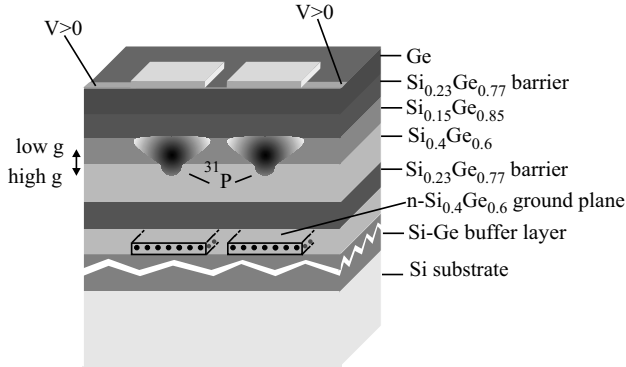


FIG. 8. Attracting the electrons to the  $\text{Si}_{0.23}\text{Ge}_{0.77}$  B-barrier reduces their Coulomb binding energy and increases their wave function overlap, allowing 2-qubit interaction.

As the electrons overlap, they will interact through the exchange interaction. It was already shown by DiVincenzo [32], that the exchange interaction can produce CNOT quantum gates.

The gate bias voltage range for 2-qubit entanglement, is indicated by the second curly bracket in Figure 4. That voltage range attracts the electrons away from the positive ions and toward the  $\text{Si}_{0.23}\text{Ge}_{0.77}$  B barrier, thus increasing their wave function overlap. In the mid-voltage range, the first curly bracket in Figure 4, 1-qubit rotations take place. Thus both one- and two-qubit interactions can be controlled by a single gate. Gate tuning of a 2-qubit exchange interaction is illustrated in Figure 8.

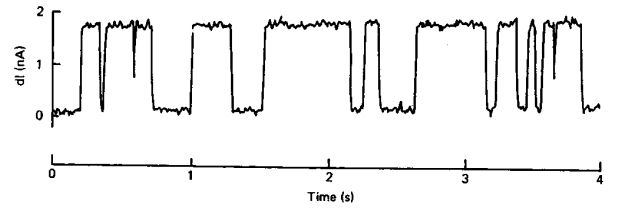


FIG. 9. The current noise in a small FET at 83 K from Kurten *et al* [34]. At this temperature the channel current fluctuates between two states, caused by a single trap being filled and emptied by a single charge. The change in channel current is  $\approx 2$  nAmps, which represents a few percent of total channel current, and is easily measured.

## VI. DETECTION OF SPIN RESONANCE BY A FET TRANSISTOR

It is a truism of semiconductor electronics that we need crystals of high perfection and extraordinary purity. Semiconductor devices are very sensitive to the presence of chemical and crystallographic faults down to the level of  $10^{11}$  defects/cm<sup>3</sup> in the volume, and  $10^8$  defects/cm<sup>2</sup> on the surface. Such defect concentrations are far below the level of sensitivity of even the most advanced chemical analytical instruments. These imperfections influence the electrical characteristics of semiconductor devices, as they vary their charge states. Thus conventional electronic devices are sensitive to very low concentrations of defects.

The detection sensitivity becomes particularly striking when the electronic devices are very tiny, as they are today. If electronic devices are small enough, then there is a good probability that not even one single defect might be present in, or on, the device. That helps define the potential yield of essentially perfect devices. But if a defect were to be present, it would have an immediate effect on the current-voltage (I-V) characteristics of that device. Therefore, the new world of small transistors is making it relatively easy to detect single defects, as their charge states directly influence the I-V curves.

As Kane pointed out, the essential point for us is to detect spin, not by its miniscule magnetic moment, but by virtue [16] of the Pauli Exclusion Principle. A donor defect can bind [33] a second electron by 1 meV, provided that second electron has opposite spin to the first electron. Thus spin detection becomes electric charge detection, the essential idea [32] behind Spin Resonance Transistors. In a small transistor, even a single charge can be relatively easily monitored.

A fairly conventional, small, Field Effect transistor, (FET) is very capable of measuring single charges, and therefore single spins as well. A single electronic charge, in the gate insulator, can have a profound effect on a low temperature FET. At more elevated temperatures for example, the motion of such individual charges produces telegraph noise in the FET channel current. An illustration of such single charge detection [34] is in Figure 9. A single electrostatic charge can add 1 additional carrier to the few hundred electrons in a FET channel. However the 2 nAmp change in channel current seen in Figure 9 represents a few percent change, and is caused by long

range Coulomb scattering influencing the resistance seen by all the electrons. At low FET operating temperatures,  $\approx 1\text{K}$ , the random flip-flops disappear, but the sensitivity to single charges remains [35].

In our spin-resonance transistor design, shown in Figures 7 and 8, the FET channel is labeled as the  $n\text{-Si}_{0.4}\text{Ge}_{0.6}$  ground plane counter-electrode. It is located under the  $^{31}\text{P}$  qubit donor, and in turn, the donor is under the top surface gate electrode. Thus the spin qubit is sandwiched between two electrodes. As in a normal FET the gate electrode modulates the  $n\text{-Si}_{0.4}\text{Ge}_{0.6}$  channel current. The qubit electron donor is positioned in the gate insulator region where its charge state can have a strong influence on the channel current. Thus the successive charge states: ionized donor, neutral donor, and doubly occupied donor ( $\text{D}^-$  state) are readily sensed by measuring the channel current.

In Figures 7 and 8, the two transistors have separate sensing channels under each transistor, so that they can be separately monitored, or indeed monitored differentially. By adjusting the gate electrodes, both qubit donor electrons can be attracted to the same donor. If they are in the singlet state they can join together forming the  $\text{D}^-$  state on one of the two dopant ions, but in the triplet state they could never occupy the same site.

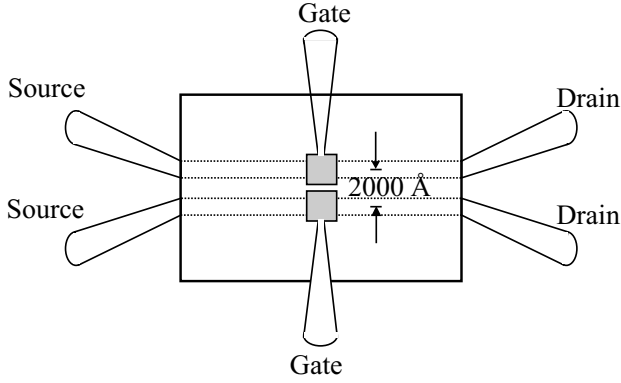


FIG. 10. Top view of the proposed CNOT gate. A perspective view (, not including the source and drain,) is shown in Figure 7.

Since the  $\text{D}^-$  state forms on one transistor, and an ionized donor  $\text{D}^+$ , on the other transistor, there would be a substantial change in differential channel current to identify the singlet state. For the triplet state, both donors remain neutral and differential channel current would be constant. As indicated by the caption to Figure 9, we can anticipate a few percent change in FET current associated with the singlet spin state, making spin readily detectable.

## VII. SMALL SCALE DEMONSTRATION

A possible 2-qubit demonstration device is shown in Figure 10. The differential current between the two FET's channels in Figure 8 would monitor the electron spin resonance. In practice a large number of transistor pairs would be arrayed

along the two FET channels in Figure 10, to allow for a finite yield in getting successful pairs.

There are two levels of doping in our proposed device: The first level of doping is the conducting FET channel doping, that needs to be at a heavy concentration to overcome freeze-out at low temperatures. This is a standard design technique in low temperature electronics. The second level of doping is in the qubit layer, that allows only one donor ion per transistor. Both doped regions need to be spatially patterned. The doped layers can be implemented by conventional ion-implantation through a patterned mask, possibly with an intermediate epitaxial growth step to minimize ion straggle. Conventional annealing can be used to remove ion damage.

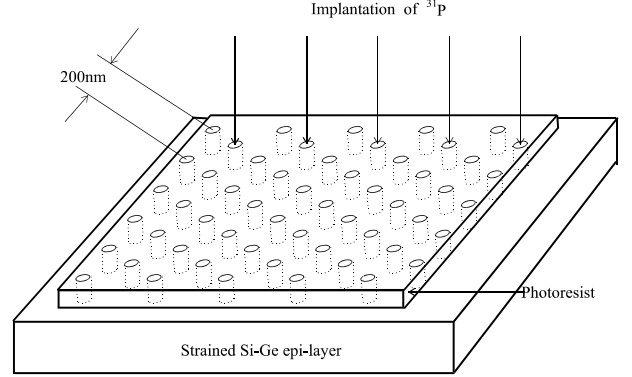


FIG. 11. The ion implantation step for inserting an array of qubit donor ions. The buried FET channels, that act as counter-electrodes to the gates and sense the spin/charge state, would be produced the same way. In a small-scale demonstration, the array would consist of only 2 rows, aligned with the FET channels of Figure 10. This should provide an adequate yield of good qubit pairs.

The ion-implantation dose for the qubit layer would be adjusted so that on average, only 1 Phosphorus ion would fall into each opening in the photoresist layer of Figure 11. By Poissonian statistics, the probability of getting exactly 1 Phosphorus ion is 36.7%. Thus the probability of getting two adjacent gates to work would be 13.5%. That is adequate yield for a small-scale two-qubit demonstration device. To improve the yield for scale-up, there are many options. For example, the dopant could be sensed by its electric charge, and re-implanted if it were absent.

## VIII. SCALING UP

There are a number of potential problems in scaling to a large computer. The future usefulness of electron spins will depend heavily on the favorable homogeneous  $T_2$  spin echo linewidth [23] in Silicon, only  $10^3\text{Hz}$ . The  $T_2$  lifetime in Si-Ge alloys has not been measured, and it will have to be demonstrated that it is as favorable as in pure Silicon. On the other hand there also appear to be methods such as isotopic purification, whereby this linewidth can be improved, particularly for well-isolated electrons.

In very large arrays, there are problems associated with the implantation yield of qubit donors. Poissonian statistics gives a yield of 36.7%, while a yield of 50% will be required for percolation, or quantum connectivity, through the two-dimensional array. There have been numerous non-Poissonian doping schemes proposed including sense/re-implant, self-assembly of molecular dopants, and scanning probe writing. Innovative doping methods have a long history, and we should anticipate that a suitable method will be optimized in time for scale-up to large quantum computers.

The other scale up issue revolves around the fact that each transistor will not be identical. As Kane noted, the transistors will have to be checked and calibrated repeatedly for use in a full-fledged quantum computer. The reason is that the nuclear spins, although almost static, will be different for each transistor. In addition the local alloy structure is different near every donor. We should not be discouraged by this checking and calibration requirement. In manufacturing classical integrated circuits, testing and repair are the biggest expense. It is common to have only a finite yield of good devices, and to reroute wiring around bad transistors. This is probably inherent in the manufacture of any large-scale system.

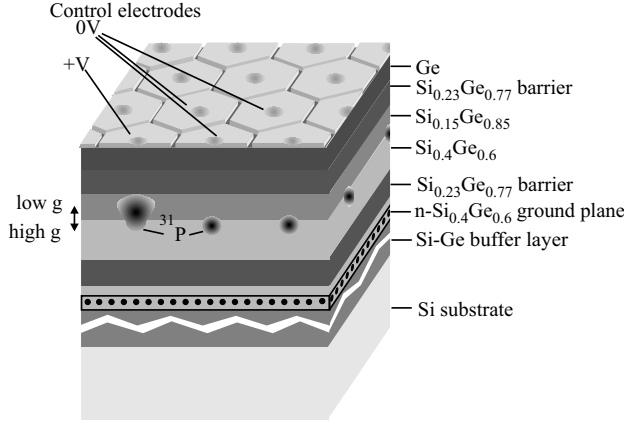


FIG. 12. In the future, we can expect arrays of Si-Ge SRT transistors. The center-to-center spacing would be  $\approx 2000\text{\AA}$ . The gate electrodes on top will perform both single and 2-qubit operations, and can be used for data and instruction read-in.

The size of spin resonance transistors, the required defect density, the increasing use of Si-Ge alloys, are all near to the present state of technology. If the spin resonance transistor (SRT) is successfully developed, we can anticipate arrays of qubits appearing much as in Figure 12.

The read-out of data requires that the buried counter electrode, opposite the gate, should also function as an FET channel. In a quantum computer, the result of the quantum computation is usually displayed on a small sub-array of all the qubits. Hence the read-out qubits can be located at the edge of the array. Figure 13 shows a qubit array, with read-out FET channels (counter-electrodes) buried under the peripheral qubits of the array. A single buried FET read-out channel can serve many qubits, since a chosen qubit can be selected

for readout by its gate electrode.

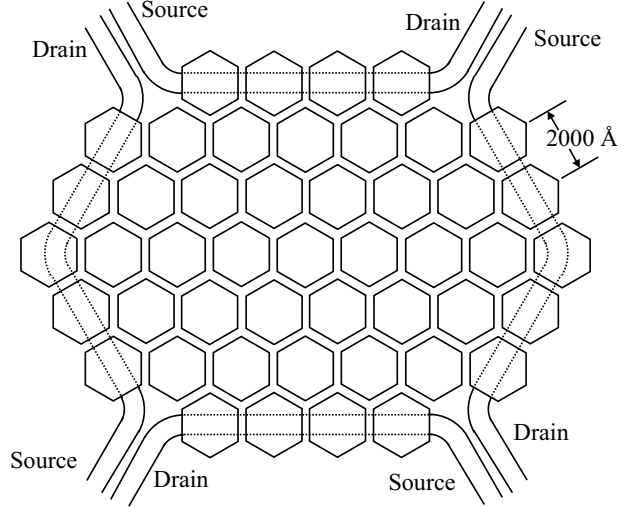


FIG. 13. In a large array, the read-out qubits would be located around the periphery. Buried FET channels would sense the spin/charge state of a selected qubit. The channel current can change by a few percent in response to a single electronic charge.

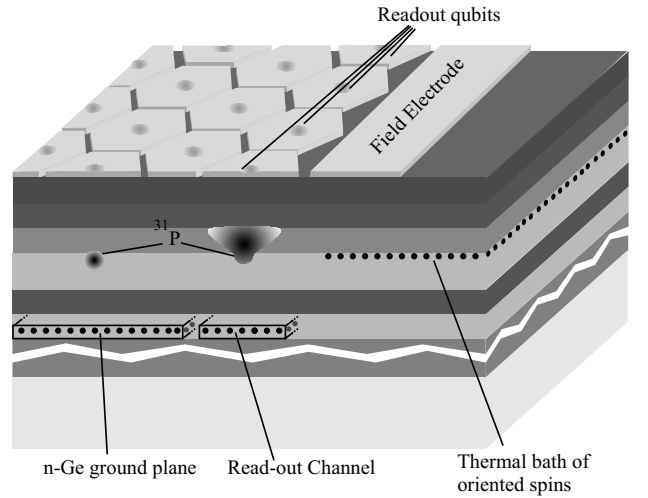


FIG. 14. A perspective view of Figure 13, gives more details of the readout architecture for the peripheral qubits. The field electrode allows the Readout Qubits to interact with the heat bath of oriented electron spins

The read-out operation can be expedited if there is a thermal reservoir of donors surrounding the peripheral qubits as shown in Figure 14. These can be attracted by a field electrode to the  $\text{Si}_{0.23}\text{Ge}_{0.77}$  B-barrier under the electrode, forming in effect a modulation doped layer. Since the operating temperature of the computer is such that  $kT \ll E_z$  with  $E_z$  the Zeeman energy of the electron spins, these qubits would be oriented by the magnetic field, and would act as a spin heat bath of known orientation. By attracting those bath



spins to a peripheral read-out qubit gate electrode, a singlet state could be formed, sensing that the readout qubit had been flipped. The current in the FET channel would then change, completing the read-out operation.

After readout, the gate voltage could be made even more positive, and the read-out qubit could thermalize with the surrounding heat bath. In effect, this resets the initial state of that peripheral qubit, which could then be swapped into the interior qubits for re-use as fault correcting ancilla qubits.

Without a doubt there will be many other issues regarding scale-up. Semiconductors, particularly Silicon, provide a track record of being tractable, engineerable materials in which many difficult accomplishments have become routine.

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